

PATENT**E3755-00002****III. Remarks****A. Objection to the Drawings**

The Action objects to Figure 1, stating that it should be labeled as "Prior Art" because only that which is old is illustrated. Applicants have made no statement in its application to the effect that the LDMOS device of FIG. 1 is prior art. Further, to the best of Applicants' knowledge, Applicants submit that no individual piece of art of record provides a device having each feature of FIG. 1 showing that FIG. 1 is prior art. For at least these reasons, reconsideration and withdrawal of the objection to FIG. 1 are respectfully requested.

B. Withdrawn Claims 26-34

In the Action, the Examiner concludes that previously added Claims 26-34 are directed to an invention that is independent or distinct from the invention originally claimed. The Examiner cites to MPEP 821.03 and 37 CFR 1.142(b) as authority. Reconsideration and withdrawal of the restriction are respectfully requested.

MPEP 821.03 states that claims added by amendment following an action should be treated in accordance with Rule 1.145. Rule 1.145 states that "[i]f, after an office action on an application, the applicant presents claims directed to an invention distinct from and independent of the invention previously claimed, the applicant will be required to restrict the claims to the invention previously claimed if the amendment is entered, subject to reconsideration and review as provided in §§ 1.143 and 1.144." Applicants submit that Claims 26-34 are not "directed to an invention distinct from and independent of the invention" under the rule and thus should not be subject to restriction and withdrawal.

The Examiner concludes that Claim 26 is directed to an invention "that is independent and distinct from the invention originally claimed" because Claim 26 has the limitation "an implant region of the first conductivity type formed at least adjacent an upper surface of said semiconductor layer and at least laterally adjacent and contacting said first source/drain region, said implant region extending laterally in a direction opposite the second source/drain region."

PATENT**E3755-00002**

Applicants submit that this feature is directly related to features that were already claimed in the original claims and are, therefore, do not make Claim 26 independent and distinct so as to impose any undue burden on the Examiner in examining them.

For example, original claim 1 recited the “silicide layer [is] formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate.” Claim 2 recited that “the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.” In combination, these claims recite (i) regions of opposite conductivity that are adjacent and connected (i.e., the first source/drain region comprising an n-type regions and p-type region (Claim 1)), (ii) the implant regions are proximate the upper surface of the substrate (i.e., the silicide layer is formed on and in electrical connection with the first source/drain region (Claim 1), and substantially proximate the n-type and p-type regions (Claim 2)), and (iii) the implant region extends laterally in a direction opposite the second source/drain region (i.e., the silicide layer is formed on and in electrical connection with the first source/drain region (Claim 1) which is substantially proximate the n-type and p-type regions (Claim 2) and extends laterally away from the gate (Claim 1).”

For at least this reason, it is submitted that, though not identically stated, the concepts claimed in Claim 26 sufficiently overlap with those originally claimed in the application such that Claim 26 is not “directed to an invention distinct from and independent of the invention previously claimed” so as to warrant restriction under Rule 1.145. It is further submitted that refusing examination of these claims denies Applicants a fair opportunity to prosecute their invention and respond to the previous Action under Rule 1.111 and Rule 1.112.

The Examiner also concludes that the “trench sinker” feature claimed in dependent Claims 28 and 29 renders these claims independent or distinct from the invention originally claimed. Again, Applicants respectfully disagree. Claim 9, for example, recites that the device

PATENT**E3755-00002**

is a lateral DMOS device. Such devices are often formed in a semiconductor epitaxial layer formed over a substrate. In order to make an electrical connection between the semiconductor layer and the substrate, trench sinkers are employed. Indeed, a trench sinker is shown in FIG. 1 of the application cited by the Examiner in the objection to the drawings. It is submitted, therefore, that these claims are not directed to an invention distinct from and independent of the invention previously claimed within the meaning of Rule 1.145.

Per the foregoing, reconsideration and withdrawal of the restriction of Claims 26-34 are respectfully requested. Examination and allowance of these claims are respectfully requested.

C. Rejection under 35 U.S.C. §102

The Action purportedly rejects Claims 1-18 as being anticipated by U.S. Published Application No. 2003/0218209 to D'Anna et al. (D'Anna). It is assumed that the Examiner intended to reject Claims 1-9, as Claims 10-18 have been canceled. Reconsideration and withdrawal of this rejection are respectfully requested in view of the following arguments.

Applicants would like to note that in the previous Action, the previous Examiner relied on U.S. Patent No. 6,521,923 to D'Anna et al., which includes FIGS. 1-5 in common with the D'Anna published application.

Applicants reserve the right to pursue the original subject matter of Claim 1, but in order to expedite the prosecution of the present application, Claim 1 has been amended to recite the features of dependent Claim 2, with slight modifications. Claim 1 now recites that the first source/drain region comprises an n-type region and a p-type region formed adjacent to said n-type region and extending laterally away from said gate, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

Providing a silicide layer on the source/drain region that extends away from the gate (i.e., parallel to the upper surface of the semiconductor layer) that forms a low resistance electrical

PATENT**E3755-00002**

path in parallel with the path formed between laterally adjacent n-type and p-type regions of the source/drain region provides several advantages that cannot be achieved by the device of D'Anna. For example, this design allows for the minimization of the lateral dimension of the N+ region of the source/drain region, so as to minimize the capacitance between contacts and the source/drain region. A P+ region extends laterally from the gate, and thus from the N+ region, providing a large available surface for forming a silicide layer through which current can be conducted from the source/drain region to a point remote from the gate, such as to a trench sinker contact to the substrate. Further, an insulator layer can be found on the silicide layer to reduce the gate-to-source capacitance, which adversely affects the high frequency performance of the device.

It is submitted that D'Anna does not teach this claimed feature.

In FIG. 3, D'Anna shows an N++ source/drain region 74 with a P body region and enhanced contact region 72 formed under the N++ region. The N++ region extends laterally to a tungsten plug 74, which may also be a "silicided plug," formed through the layer 56 to the substrate. Any portions of the plug 76 formed over the semiconductor layer 76 do not form an electrical connection that is parallel to the current path (if any) between the N++ region and P regions. Focusing on FIG. 3, it is clear that D'Anna's structure, therefore, does not include a first source/drain region comprising an n-type region and a p-type region formed adjacent to said n-type region and extending laterally away from said gate, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

For at least these reasons, it is submitted that Claim 1 and Claims 3-9, which depend from Claim 1, are not anticipated by D'Anna and are allowable over the art of record.

Claim 3 has been amended consistent with the amendments to Claim 1.

PATENT**E3755-00002**

Claim 19 has been amended to recite that the MOS device further includes an implant region having conductivity opposite the first source/drain region having a region proximate the upper surface of said semiconductor layer extending laterally away from the gate. The claim also recites that substantially all of the current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to said implant region. Some of these features can be found in original Claim 21, which has been canceled, accordingly.

As argued above, the N++ region of D'Anna extends directly to the plug 74. The structure of D'Anna does not include an implant region having a conductivity opposite the first source/drain region having a region proximate the upper surface of said semiconductor layer extending laterally away from the gate such that substantially all of the current associated with the first source/drain region would pass through the silicide layer in a direction from the first source/drain region to said implant region.

For at least this reason, it is submitted that Claim 19 and Claims 20 and 22-25, which depend from Claim 19, are not anticipated by and are allowable over D'Anna.

Claim 20 has been amended consistent with the amendments to Claim 19.

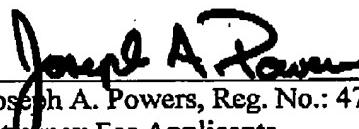
In view of the foregoing amendments and arguments, reconsideration and withdrawal of the rejection of the claims are respectfully requested.

PATENT**E3755-00002****IV. Conclusion**

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

Dated: 6/16/06

Joseph A. Powers
Reg. No.: 47,006
Attorney For Applicants

DUANE MORRIS LLP
One Liberty Place
Philadelphia, Pennsylvania 19103-7396
(215) 979-1842 (Telephone)
(215) 979-1020 (Fax)